Technical Details for Meity's C2SD Project

Title: The design, fabrication and development of silicon proven IP Core for high resolution ADPLL.

Motivation:

PLL is a basic building block mainly used to generate clock or carrier signals. It is extensively found in applications of wireless communication systems like Bluetooth, Wi-Fi, GSM etc. In other words, PLL is present in almost all wireless communication systems. It is difficult to imagine a wireless communication system without a PLL. It must be noted that present SoCs which are designed for smartphones, smart watches, etc., have Bluetooth and Wi-Fi IP cores embedded into their SoCs. Hence, there exist a huge demand for these IP cores. But some issues that are usually encountered with these IP cores is their large area, high power consumption and the effect of PVT variations. Therefore, the present research in this field is to replace the conventional analog PLLs with all digital PLLs (ADPLLs). ADPLLs are designed using digital logic and hence can have advantages like small area, lower power consumption and immunity to PVT variations.

However, one issue that seriously hinders the use of ADPLLs is its bad resolution and high spurs. ADPLLs are known to have very bad phase noise performance compared to analog-PLLs, thereby restricting their prospective. But there is an immense research being done to improve its resolution and phase noise performance of ADPLLs . Lately, new architectures of ADPLLs have been developed that can immensely improve the resolution and phase noise performance of ADPLLs.

Hence, in this work we propose to design and fabricate a high-resolution, low phase noise ADPLL IP core for Bluetooth Low energy applications. As already mentioned earlier, due to its digital implementation it can provide advantages of small area, low power consumption and immunity to PVT variations. Once, fabricated we will be possessing a silicon proven IP core of such an advanced ADPLL which will attract SoC manufacturers from all corners of the world and provide huge potential for commercialization. It will revolutionize the design of communication radio in semiconductor industry.

Introduction:

PLL is the basic building block of many ICs and systems. It has many applications like phase locking, frequency synthesis, clock synthesis, carrier generation, etc. A PLL consists of three

blocks i.e. a Phase Detector, an LPF, and a VCO, as shown in the Figure-1. . The Phase detector detects the phase difference between the reference input and output signal and generates a dc voltage proportional to the phase difference. The output voltage of the phase detector is filtered by an LPF to produce a smooth, slow varying signal which is fed to VCO . A VCO's output frequency is proportional to the applied input voltage. This setup forms negative feedback closed loop system and ultimately PLLs will try to make any error between input and output frequency to be zero. Thereby, providing an output frequency that is equal to the reference input.

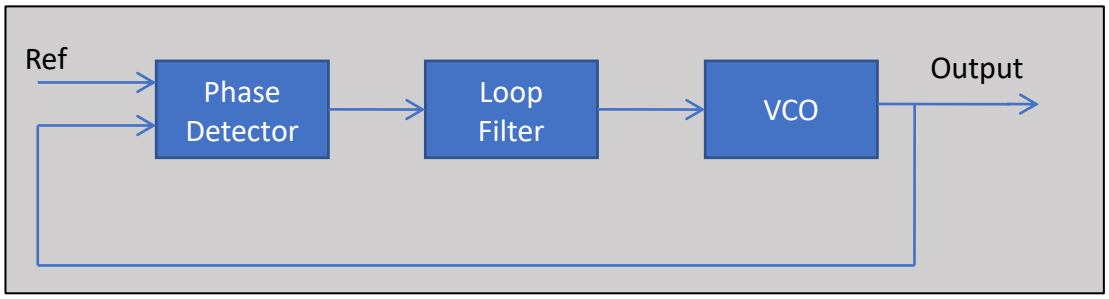

Figure 1 Block Diagram of a conventional PLL

When used as clock synthesizer or carrier generator. The feedback circuit of the PLL is modified to that of the figure-2. In this setup output frequency will be $N*f_{REF}$.

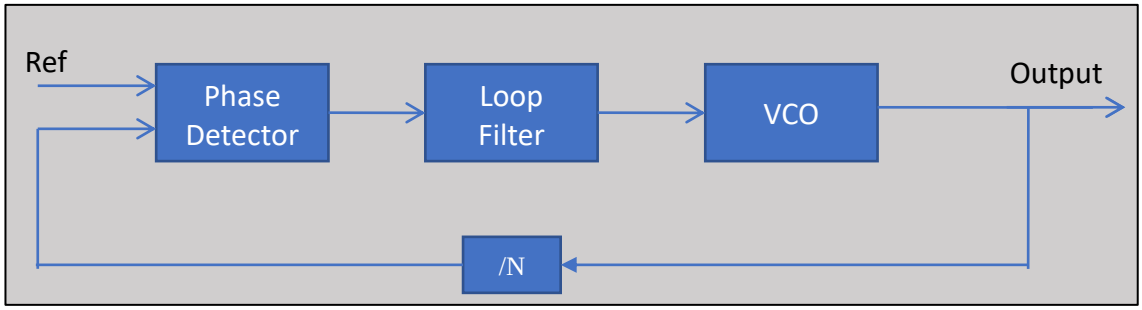

Figure 2 Block Diagram of a conventional PLL

It is possible to implement the PLL in many ways. For example, it is possible to implement PD, LPF, and VCO as analog components or all the three can be implemented in the digital domain. It is also possible to implement some of the blocks in analog and the remaining in the digital domain. It is obvious that considering all combinations, many different varieties of PLL realizations are possible. Based on their realization, these circuits are either called PLL / DPLL / ADPLLs. An All-Digital PLL (ADPLL) has all components implemented in the digital domain. i.e. PD, LPF, and DCO (in the digital implementation a VCO) are all digital circuits. Block diagram of an ADPLL is shown in the figure-1 for illustration.

With the onset of 21st century there is a rising interest in the development of all digital PLLs for generation of stable clock/carrier signal due to it's immunity to PVT variations. However, it was initially reported that though, ADPLLs can be realised in CMOS digital circuits, but their performance was not comparable to their analog counterparts [1][2]. The major challenges being resolution and phase noise performance.

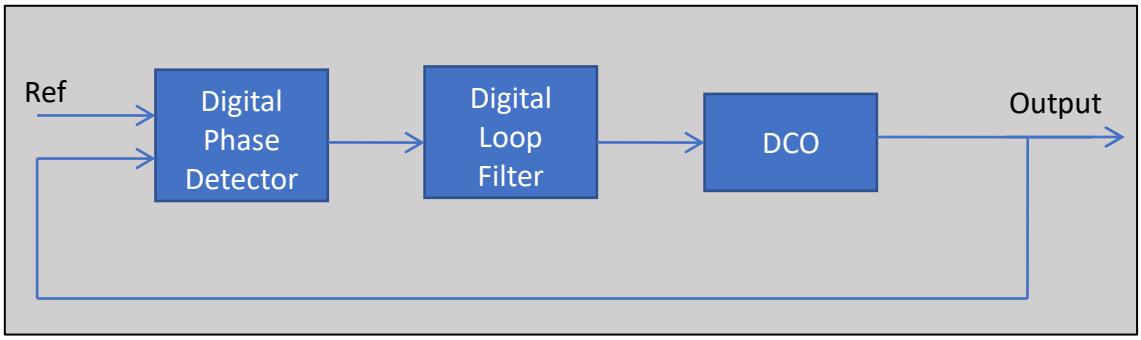

Figure 3; illustrative block diagram of an All-Digital PLL (ADPLL)

ADPLLs are however a favourable choice because of the advantages of digital circuits against PVT variations. Moreover, the digital implementations result in smaller area as compared to analog because analog PLLs require charge-pump and filter capacitors which occupy huge area and are prone to PVT variations. This advantage of smaller area and immunity to external variations have fascinated the researchers towards the development of high resolution all digital PLLs.

The delay line based TDC can provide resolution which is equal to the delay of single element which can be either a buffer or an inverter. It can be observed that such TDC could provide sub-nano second resolution. To further increase the resolution of phase- detection Vernier TDCs were developed. Increasing the resolution by using above techniques result in decrease of the linear range of the ADPLL.

Once the resolution in phase detection was achieved, the effort are made to increase the resolution of VCO. Digitally controlled VCOs were developed which worked by switching the capacitances attached to an LC oscillator or switching extra delay elements in a ring oscillator based DCO. However, the output resolution being provided by such approaches is not sufficient for most to the practical purposes. Hence many noise reduction techniques like the use of DSM and dithering are being used to increase resolution of output and decrease the phase noise.